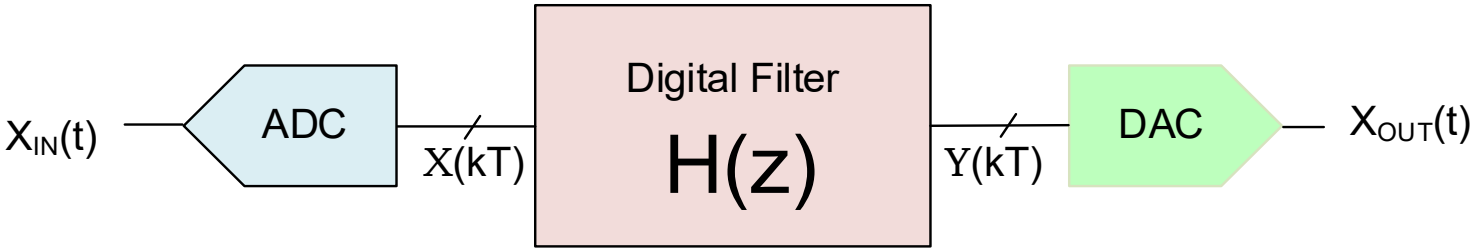
EE 508 Lecture 39

Digital/Analog Filter Comparisons
Some Recent Filter Structures

Review from last lecture

Digital Filter Properties



Theorem: Any FIR filter is linear phase if the impulse response is symmetric or antisymmetric

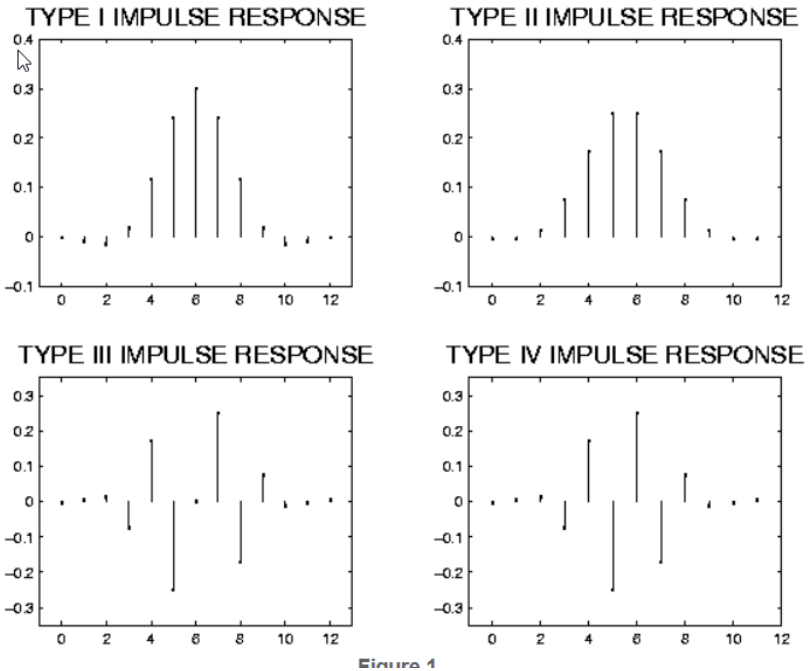
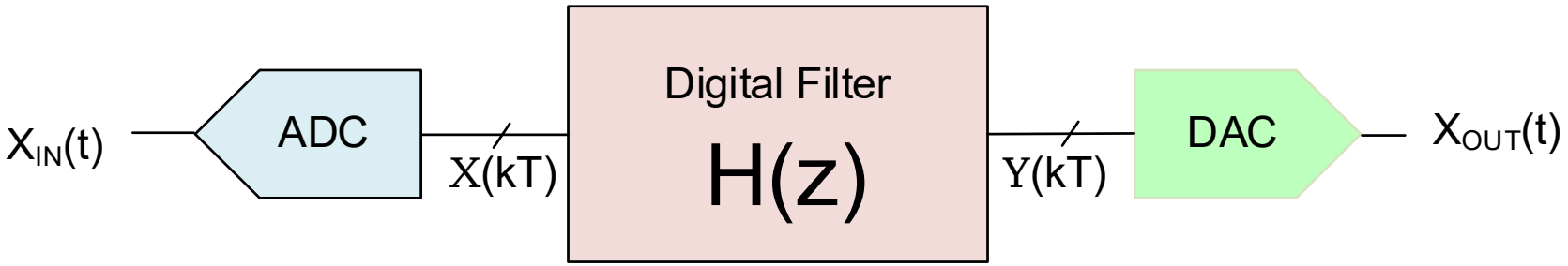


Table from Robert Novak book

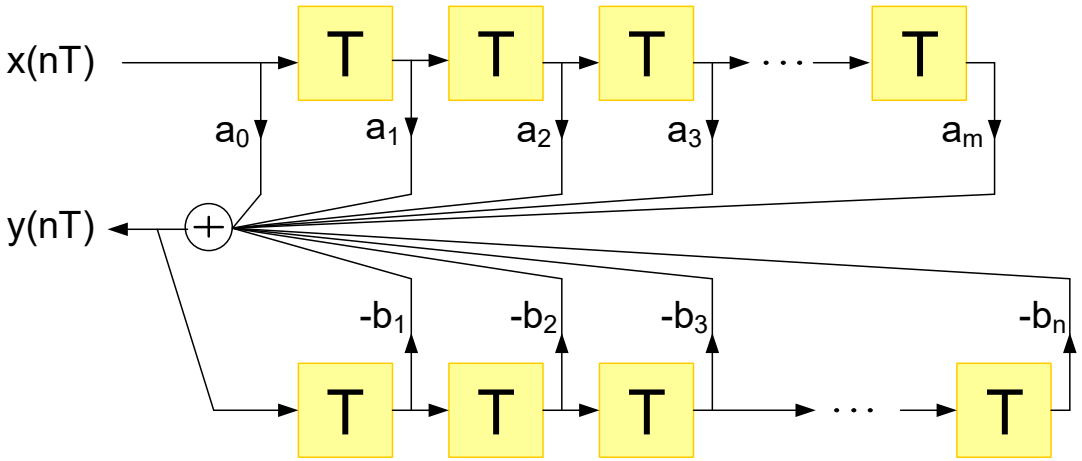
Review from last lecture

Digital Filter Properties

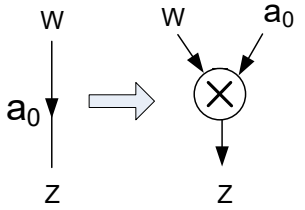


$$y(nT) = \sum_{i=0}^{m} a_i x(nT - iT) + \sum_{i=1}^{n} b_i y(nT - iT)$$

An Implementation of a Digital Filter



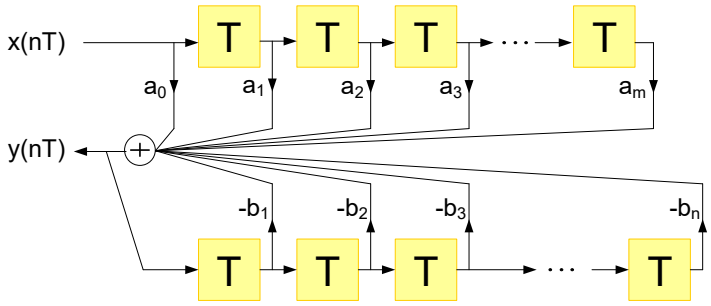
Delay Element



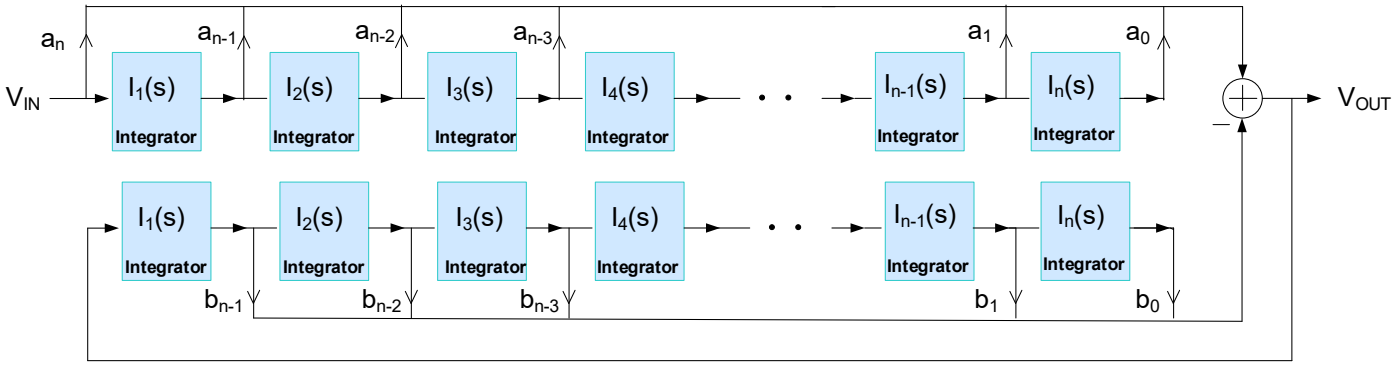
Multiply Element

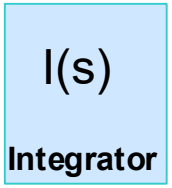
Review from last lecture

An Implementation of a Digital Filter



An Implementation of an Analog Filter

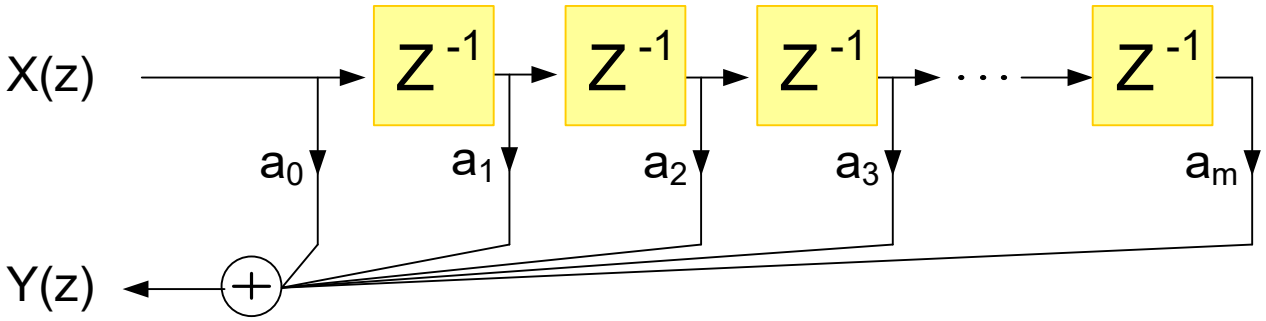


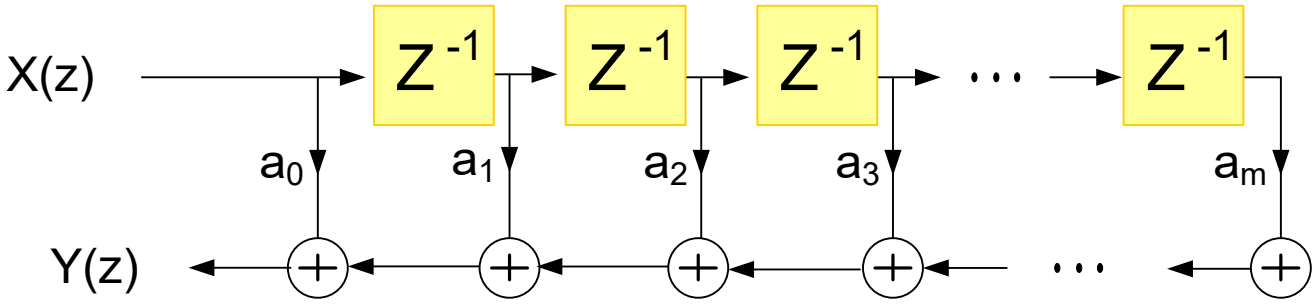


- Can be viewed as analogous implementations
- Neither particularly practical
- Many other architectures for both analog and digital filters
- Approximately double the number of integrators or delay elements needed

Review from last lecture

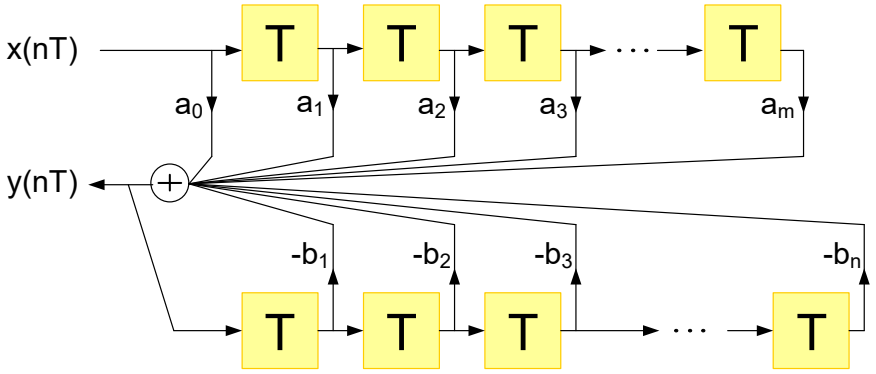
Alternate Implementations of an FIR Digital Filter

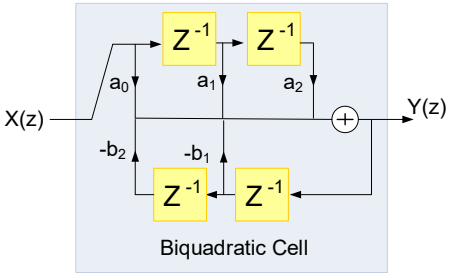


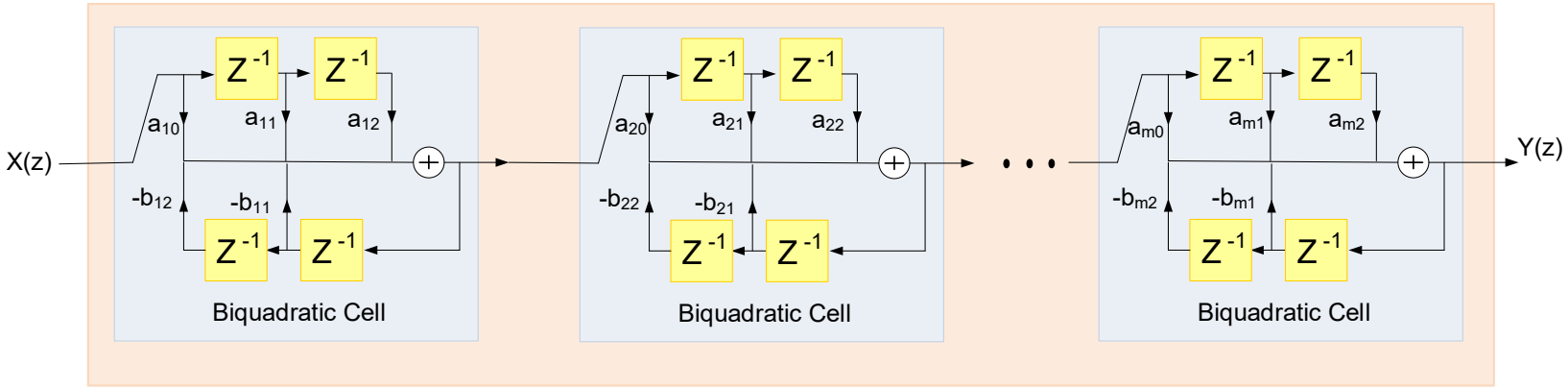


Review from last lecture

Alternate Implementations of IIR Digital Filter

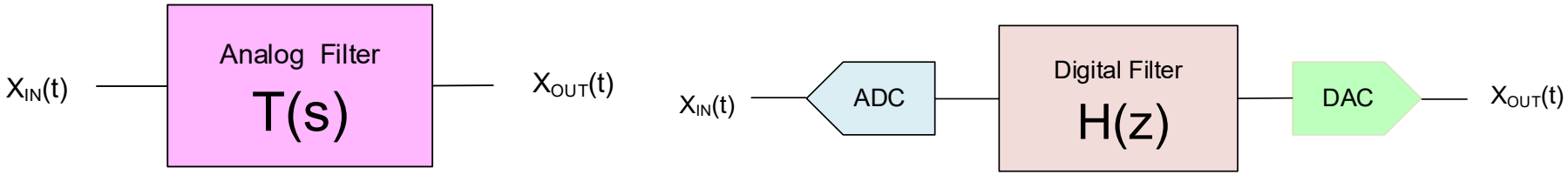






Excessive delay elements but not of as much concern as excessive Integrators

Does Digital Filter Overcome Limitations



A - Transfer functions sensitive to component and process variations

D - Transfer function part of H(z) not sensitive to process variations
- Transfer function sensitive to coefficient quantization
- ADC and DAC minimally sensitive to process variations but highly sensitive to mismatch

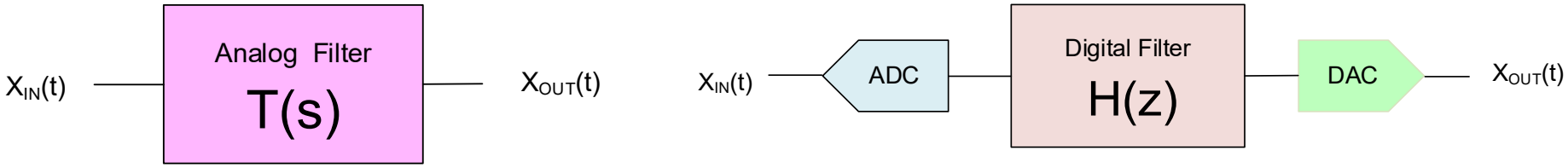
A - Distortion inherent due to nonlinearities in components (particularly amplifiers)

D - Transfer function part of H(z) not sensitive nonlinearity of components
- ADC and DAC sensitive to nonlinearity of components

A - Power dissipation can be large

D - Power dissipation can be large due to a large number of arithmetic operations during each clock cycle
- ADC and DAC dissipate considerable energy for high resolution or high speed

Does Digital Filter Overcome Limitations



A - Area gets large, often unacceptably so for very low frequency poles and even of concern for audio-frequency poles

D - Area for DSP in Digital Filter can be large
- ADC and DAC can become large if high resolution is required
- No area penalty for low frequency operation of digital system

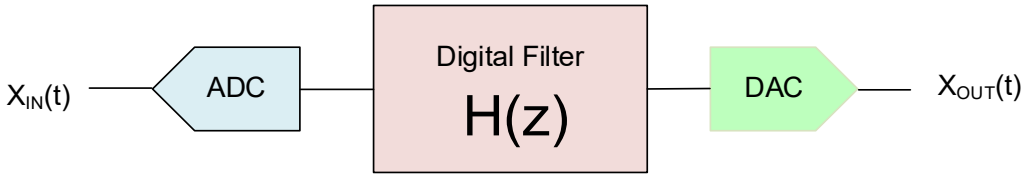
A - Programmability introduces considerable complexity (with existing approaches)

D - Programmability of filter characteristics is very efficient with digital filter approach

A - Making minor changes in filter requirements often necessitates a major redesign effort

D - Making minor or even major changes in filter requirements requires minimal effort with digital filter approach

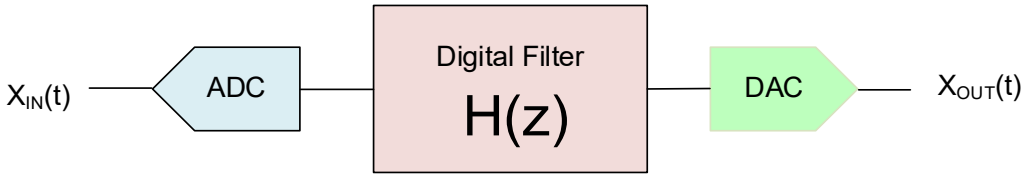
Digital Filter Design Issues

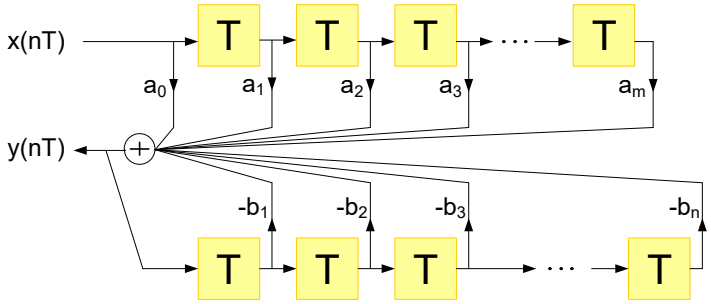


Order of Digital Filters Can be Large

- 128 or more delay elements are not uncommon
- Can achieve very steep transitions from passband to stop band
- High Q poles can be practically realized
- Particularly attractive for filtering low-frequency signals
- Large number of adds and multiplies slows response of the filter
- ARMA filters invariably are of lower order than FIR filters for given transition requirements
- FIR filters inherently stable

Digital Filter Design Issues

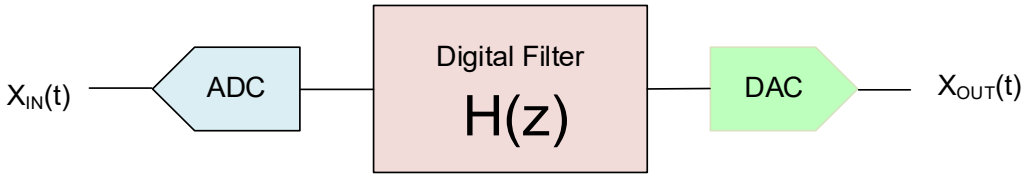


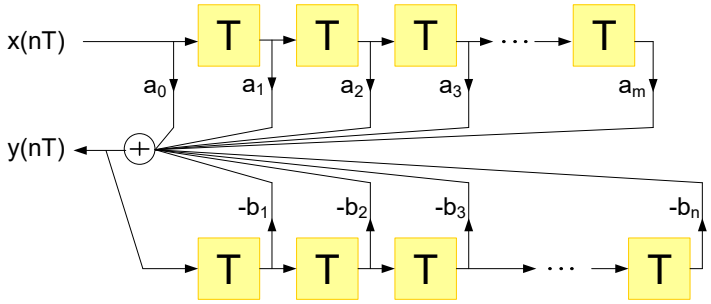


Architectural Issues

- Many different filter architectures
- Must be sure to not overflow registers during intermediate calculations
- Order of operations for given architecture can affect performance
- Coefficient sensitivity can be high
- Number of bits of resolution on coefficients affects multiply and add times
- Some work on filters where all coefficients are power of 2 (multiplies become simply shifts)
- Concerns about how many intermediate memory locations are required

Digital Filter Design Issues

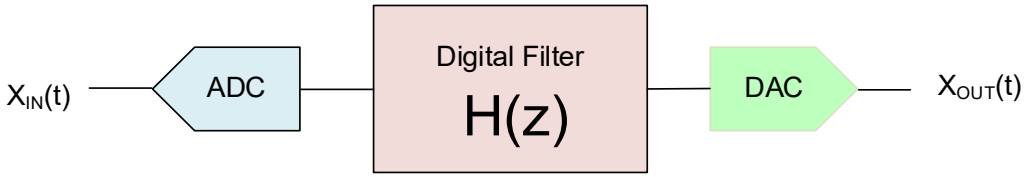


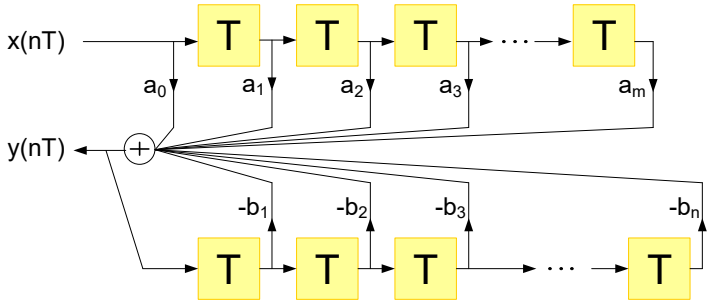


Architectural Issues

- May not be easy to assess overflow concerns without overdesign since intermediate totals dependent upon input
- Architecture affects number of arithmetic operations
- Large number of operations can introduce noise into substrate which of concern with systems with extreme SNR where ADC and DAC are on-chip
- Some architectures and some approximations naturally support parallel operations

Digital Filter Design Issues

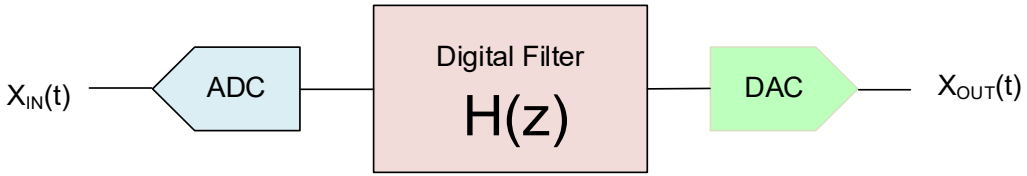


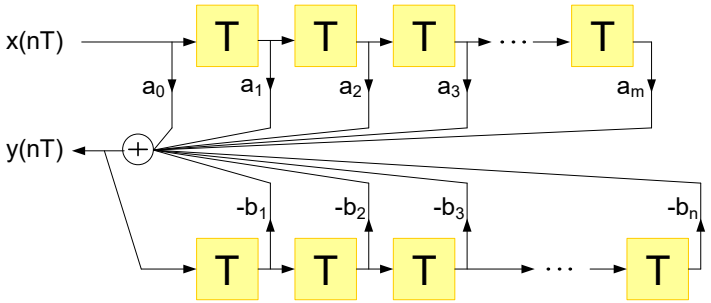


General Comments

- Extreme precision possible with right order and good implementation
- Time and amplitude quantization both affect performance
- Not practical for applications that have very high frequency poles (due to both data converter and filter limitations)
- Power dissipation can be large if many arithmetic operations are required
- May not be easy to assess overflow concerns without overdesign since intermediate totals dependent upon input
- ADC and DAC design efforts can be substantial
- ADC and DAC may require considerable area and power
- Significant effort in design of computer or DSP to drive the digital filter

Digital Filter Design Issues

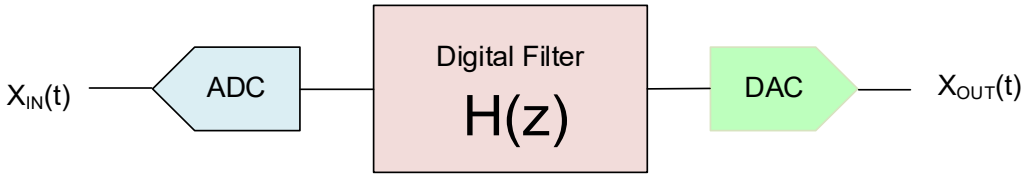


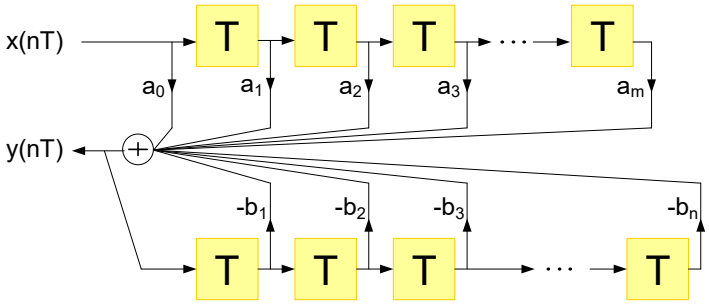


General Comments

- Though process variations in digital filter not of concern, they do affect the ADC and DAC designs beyond matching (e.g. clock skew)
- Big step in area and power to implement the DSP and filter
- Switched Capacitor filters have some properties of a digital filter (time-quantization and thus H(z) instead of T(s)) and some of analog filters but overhead for implementing a lower-order filter with SC techniques is relatively small
- DAC often not required since decisions are often made in digital logic and no subsequent analog output is required
- One (of many) applications that favor use of digital filters is in output filtering and decimation in delta-sigma ADCs

Digital Filter Design Issues

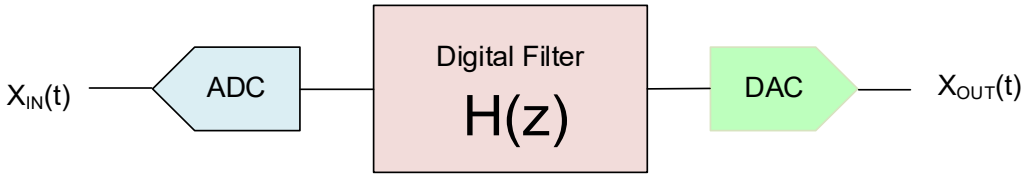


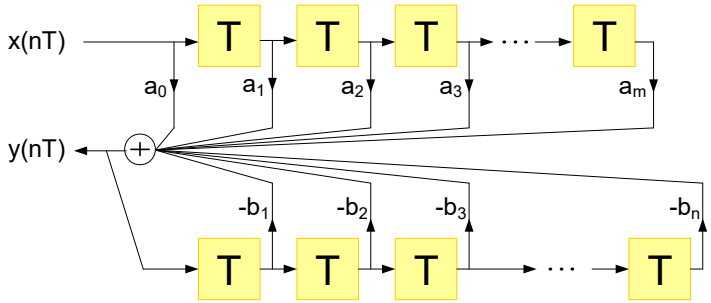


General Comments

- Digital filters are vulnerable to aliasing
- Digital filters are expensive
- Digital filters limited to relatively low frequency operation (due to both the data converters and the adds/multiplies)
- Digital filter intermediate results can be stored for later analysis
- The H(z) portion of the digital filter benefits from technology scaling
- The H(z) portion does not drift with time or temperature
- H(z) can be easily tweaked or even modified with software

Digital Filter Design Issues





General Comments

- Implementations of digital filters in FPGAs appears to be a topic of interest itself
- Digital filter design a significant component of the topic of digital signal processing
- Entire graduate level course could be dedicated to topic of digital filter design

SECTION 6
DIGITAL FILTERS

Walt Kester

COMPARISON BETWEEN FIR AND IIR FILTERS

IIR FILTERS	FIR FILTERS
More Efficient	Less Efficient
Analog Equivalent	No Analog Equivalent
May Be Unstable	Always Stable
Non-Linear Phase Response	Linear Phase Response
More Ringing on Glitches	Less Ringing on Glitches
CAD Design Packages Available	CAD Design Packages Available
No Efficiency Gained by Decimation	Decimation Increases Efficiency

SECTION 6
DIGITAL FILTERS

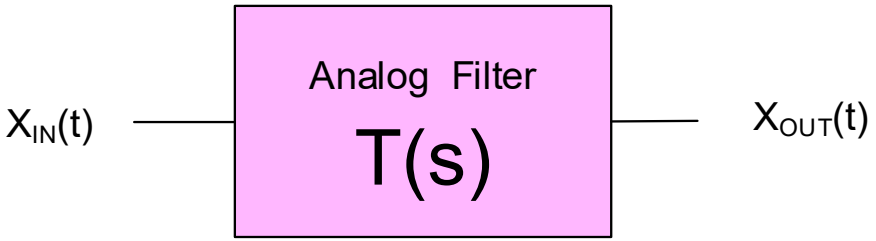
Walt Kester

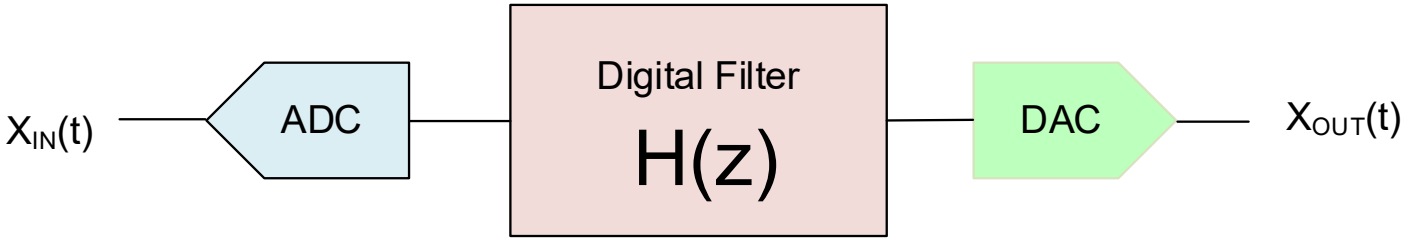
DIGITAL VERSUS ANALOG FILTERING

DIGITAL FILTERS	ANALOG FILTERS
High Accuracy	Less Accuracy - Component Tolerances
Linear Phase (FIR Filters)	Non-Linear Phase
No Drift Due to Component Variations	Drift Due to Component Variations
Flexible, Adaptive Filtering Possible	Adaptive Filters Difficult
Easy to Simulate and Design	Difficult to Simulate and Design
Computation Must be Completed in Sampling Period - Limits Real Time Operation	Analog Filters Required at High Frequencies and for Anti-Aliasing Filters
Requires High Performance ADC, DAC & DSP	No ADC, DAC, or DSP Required

Figure 6.2

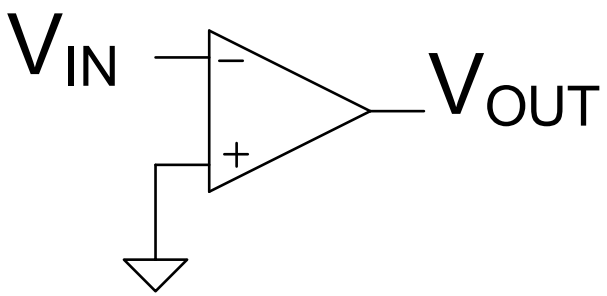
Analog vs Digital Filter





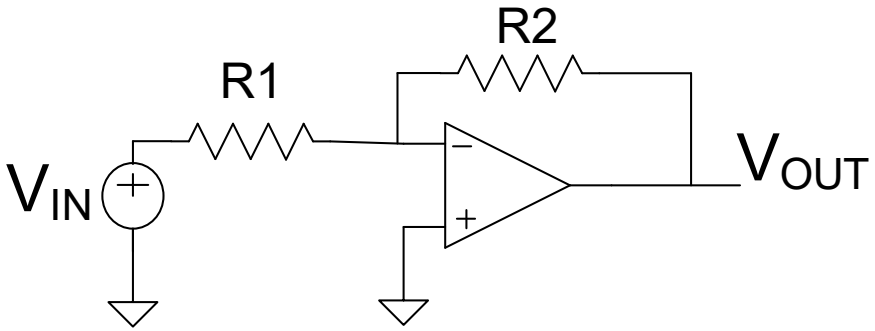
- Both approaches have advantages and limitations
- Digital filters particularly attractive if DSP already available and if ADC and DAC are necessary for other purposes or if decisions in system must be made in the digital domain
- Digital filters also attractive if much of the signal processing will occur in the digital domain of a system
- Digital filters have replaced analog filters in many applications

Op Amp or Integrator?



$$\frac{V_{OUT}}{V_{IN}} \cong \frac{GB}{s}$$

Amplifier or LP Filter or Lossy Integrator?



$$\frac{V_{OUT}}{V_{IN}} \cong \frac{-\frac{R_2}{R_1}}{1+\tau s\left(1+\frac{R_2}{R_1}\right)}$$

In about 1974 Michael Soderstrand introduced this concept for building high-frequency filters and termed these “Active-R” filters

Active R filters: review of theory and practice
JR Brand, **R** Schaumann - IEE Journal on Electronic Circuits ..., 1978 - ieeexplore.ieee.org
Active filters that derive their frequency response from internal amplifier dynamics, but use no external capacitors in their implementation, are referred to as' **active R**'**filters**. Because of their potential advantages in terms of miniaturisation (ie fabrication), ease of design and ...
☆ Cited by 101 Related articles All 3 versions Web of Science: 53

The compensation capacitor in the op amp serves as the energy storage element in the filter

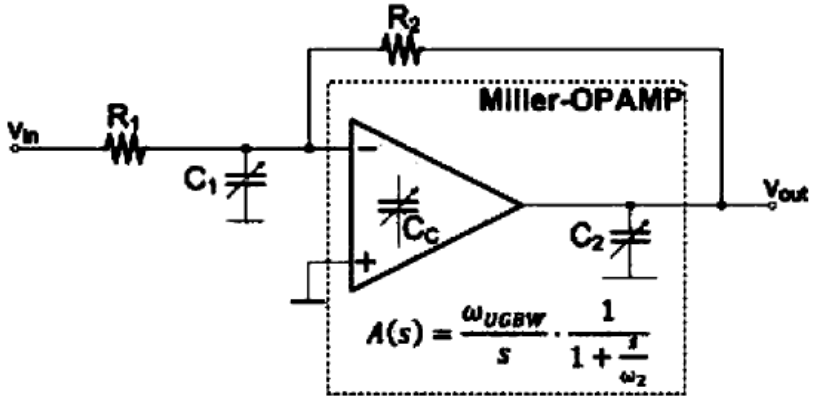
Can operate at very high frequencies but many problems with linearity and accuracy

A 0.9V 3rd-Order Single-OPAMP Analog Filter in 28nm CMOS-bulk

Marcello De Matteis[1,2], Andrea Donno[3,4], Stefano Marinaci[4], Stefano D'Amico[3,4], Andrea Baschirotto[1,2]

From IEEE Int. Workshop on Advances in Sensors and Interfaces, June 2017

"The scheme take advantage of the efficient Active-gm-RC filter [3], which exploits the Opamp unity gain bandwidth (COUGBW) to synthesize the transfer function."



g. 1 – Single ended architecture of the proposed analog filter

Tab. I – Targeted filter transfer function parameters

Parameter	This Design
ω_{23} – real pole frequency	$2\cdot\pi\cdot$350MHz
ω_0 – complex poles frequency	$2\cdot\pi\cdot$160MHz
Q_0 – complex pole quality factor	0.9
f_{-3dB}- cut-off frequency	$2\cdot\pi\cdot$132MHz
G – low pass filter dc-gain	0dB

[3] A. Donno, S. D'Amico, M. De Matteis, A. Baschirotto "A 150MHz 3rd-order single Opamp continuous-time analog filter in 28nm CMOS technology" Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2015, Cairo (Egypt); 6-9 December 2015 (DOI: 10.1109/ICECS.2015.7440274).

A 0.9V 600MHz 4th-Order Analog Filter with Feed-Forward Compensated OPAMP in CMOS 28nm F. Ciciotti, M. De Matteis, and A. Baschirotto

PRIME Conference, June 2017

"The transfer function is obtained with the cascade of two Active-RC Rauch biquadratic cells. Each cell is based on a novel OPAMP optimized for very high frequency operation achieving a Unity Gain Bandwidth (UGBW) > 7GHz."

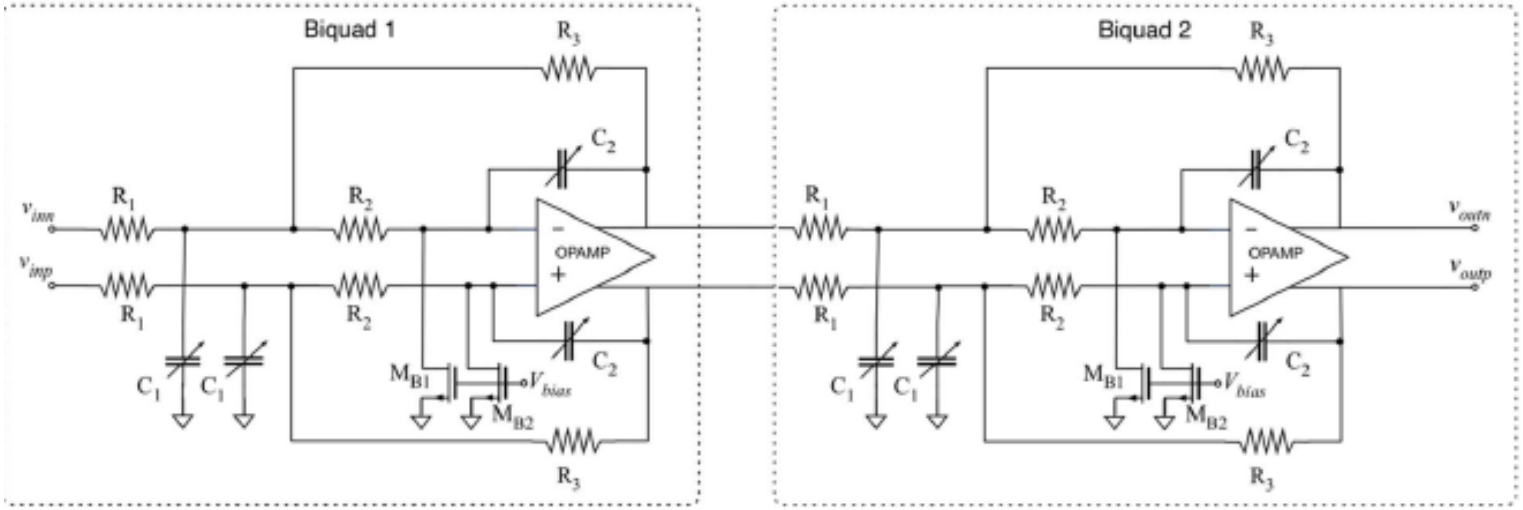
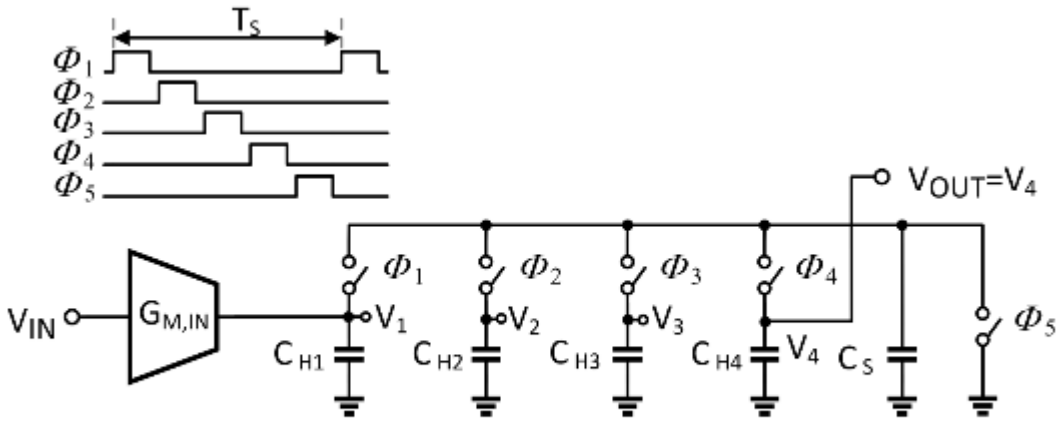


Fig. 1. Filter chain.

This is actually a bridged-T structure !

SC Filter w/o Op Amp

M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE J. Solid-State Circuits*, vl. 49, no. 11, pp. 2575–2587, Nov. 2014.



. 1. A 4^{th}-order real-pole passive-SC LPF [2].

SC Filter w/o Op Amp

S. Iida, "Filter circuit, integrated circuit, communication module, and communication apparatus," U.S. Patent 0 334 348 A1, Nov. 13, 2014.

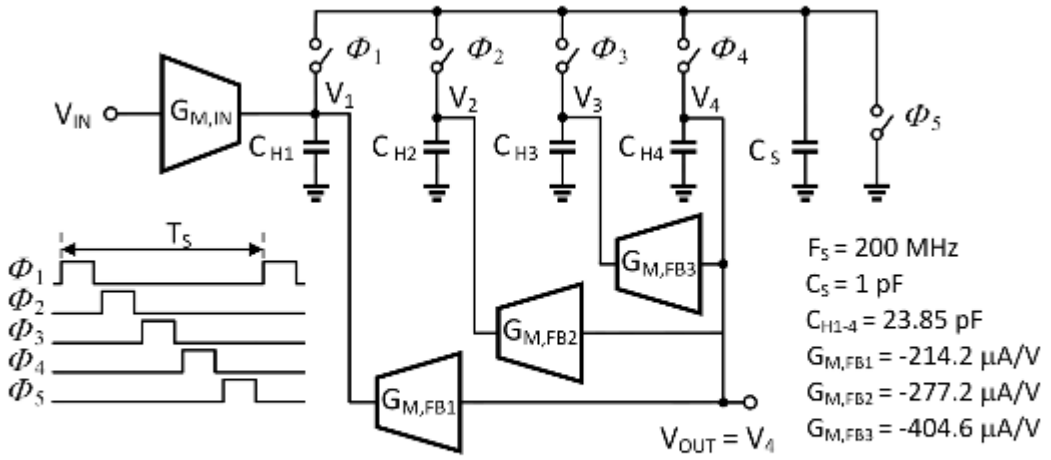


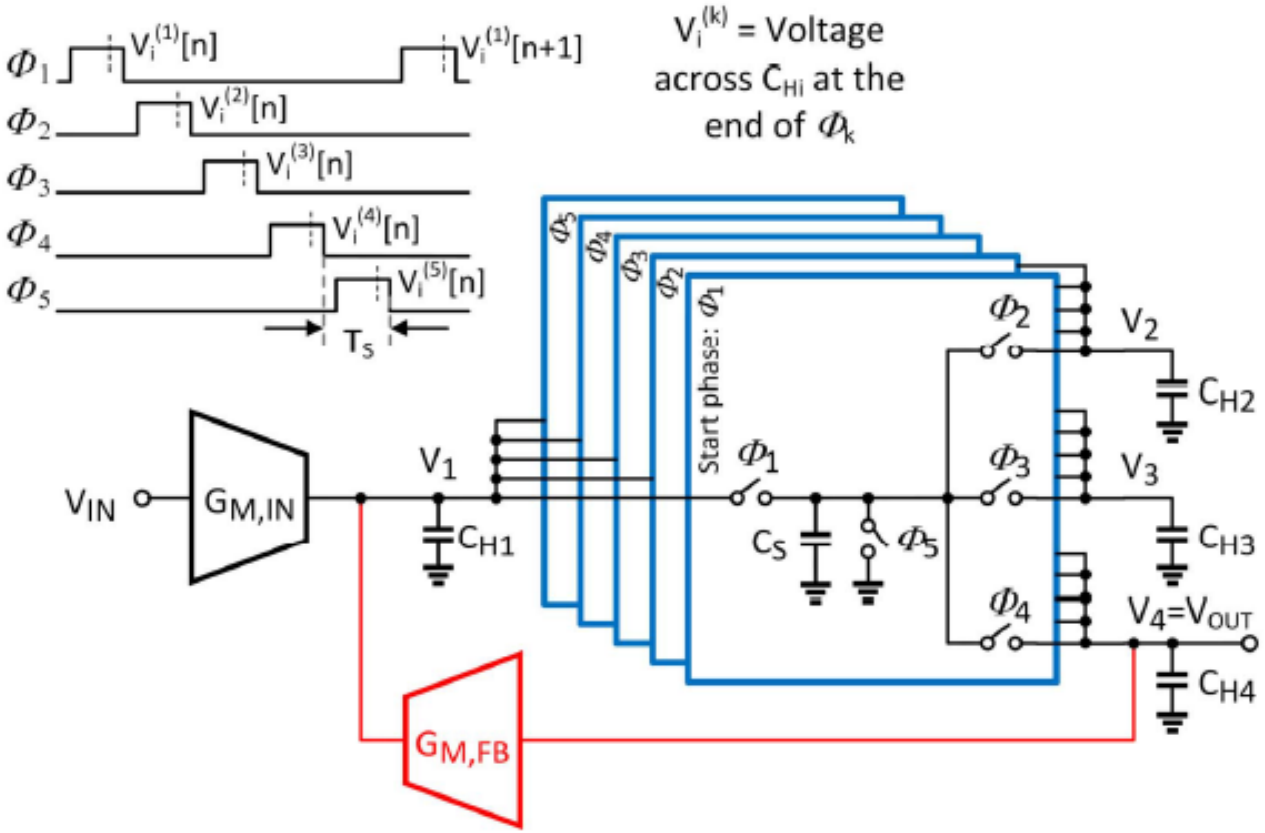
Fig. 3. A 4^{th}-order complex-pole filter [21].

SC Filter w/o Op Amp

A 0.49–13.3 MHz Tunable Fourth-Order LPF with Complex Poles Achieving 28.7 dBm OIP3

Pedram Payandehnia, *Student Member, IEEE*, Hamidreza Maghami, *Student Member, IEEE*, Hossein Mirzaie, *Student Member, IEEE*, Manjunath Kareppagoudr, *Student Member, IEEE*, Siladitya Dey, *Student Member, IEEE*, Massoud Tohidian, *Member, IEEE*, and Gabor C. Temes, *Life Fellow, IEEE*

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 65, NO. 8, AUGUST 2018

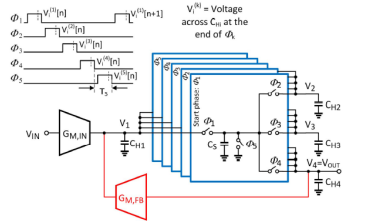


SC Filter w/o Op Amp

A 0.49–13.3 MHz Tunable Fourth-Order LPF with Complex Poles Achieving 28.7 dBm OIP3

Pedram Payandehnia, *Student Member, IEEE*, Hamidreza Maghami, *Student Member, IEEE*, Hossein Mirzaie, *Student Member, IEEE*, Manjunath Kareppagoudr, *Student Member, IEEE*, Siladitya Dey, *Student Member, IEEE*, Massoud Tohidian, *Member, IEEE*, and Gabor C. Temes, *Life Fellow, IEEE*

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 65, NO. 8, AUGUST 2018



Technology	180 nm
Order	4^{th}
VDD (V)	1.8
Power (mW)	4.3
3-dB BW (MHz)	0.49-13.3

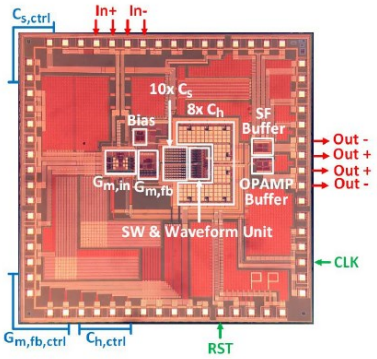
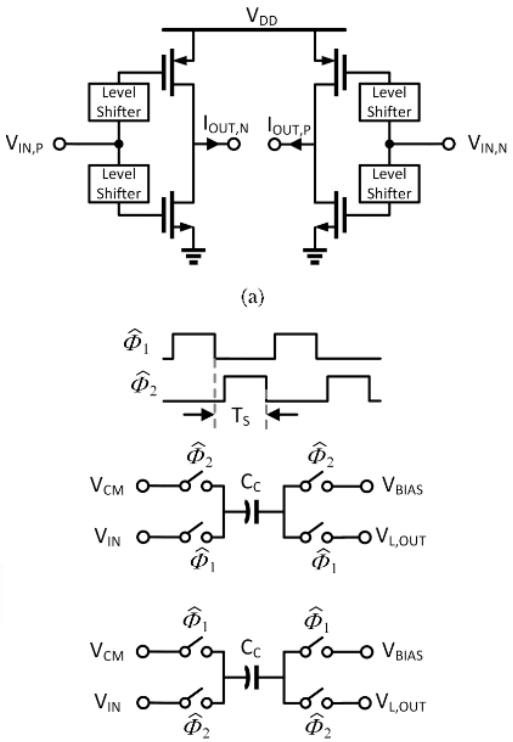
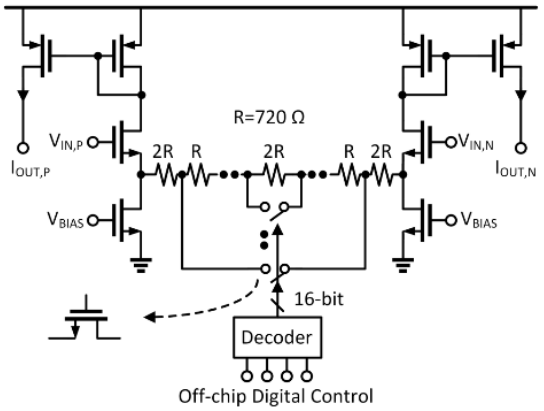


Fig. 17. Chip micrograph of the proposed filter implemented in 1P4M 180 nm CMOS technology. Die size is 4 × 4 mm.



Input OTA



Feedback OTA

A 20kHz~16MHz Programmable-Bandwidth 4th Order Active Filter using Gain-boosted Opamp with Negative Resistance in 65 nm CMOS

Jiye Lim, *Student Member, IEEE,* and Jintae Kim, *Senior Member, IEEE*

Accepted for TCAS II and pending publication Nov18

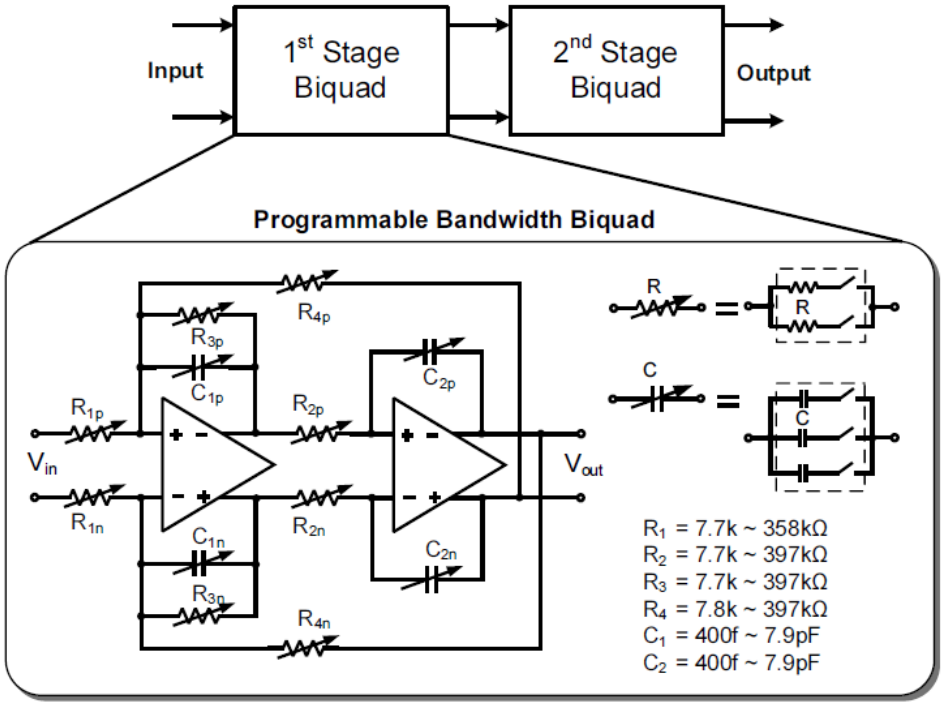


Fig. 1. A block diagram of 4th order programmable biquad filter.

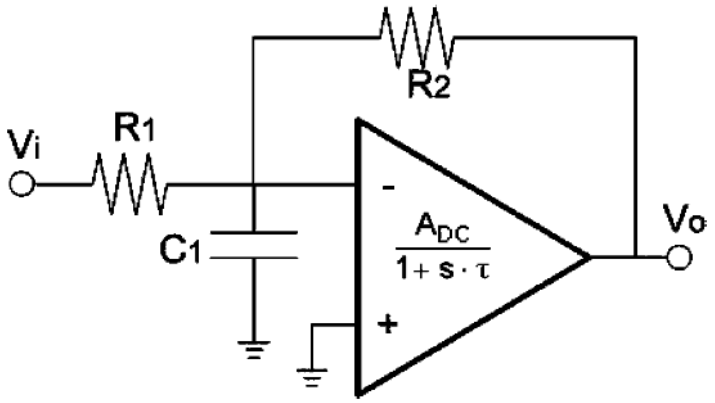
The prototype filter is fabricated in 65nm CMOS and occupies 0.098mm^2. It features three programmable cutoff frequencies of 20kHz, 2MHz, and 16MHz

Power (mW)	19

A 4th-Order Active-Gm-*RC* Reconfigurable (UMTS/WLAN) Filter

Stefano D'Amico, Vito Giannini, and Andrea Baschirotto

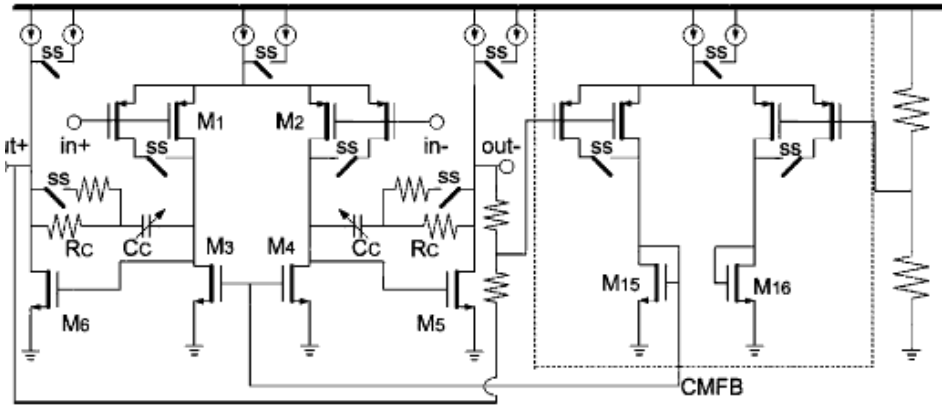
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 7, JULY 2006



$$\left.\begin{aligned} V_{IN}G_1 + V_{OUT}G_2 &= V_X\left(G_1+G_2+sC\right) \\ V_{OUT} &= V_X\frac{-A_0}{1+\tau s} \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\frac{A_0G_1}{\tau C}}{s^2 + s\left[\frac{G_1+G_2}{C}+\frac{1}{\tau}\right]+\frac{G_1+G_2(1+A_0)}{\tau C}}$$

Active-G_m-*RC* biquadratic cell.



Differential Amp

Realizes 4th-order filter

C1 and CC tunable,
R1 and R2 switchable

Operates in 2MHz and
20MHz ranges

A 28.8-MHz 23-dBm-IIP3 3.2-mW Sallen-Key Fourth-Order Filter With Out-of-Band Zeros Cancellation Marcello De Matteis, Federica Resta, Alessandra Pipino, Stefano D'Amico, and Andrea Baschirotto

TCAS II Dec 16

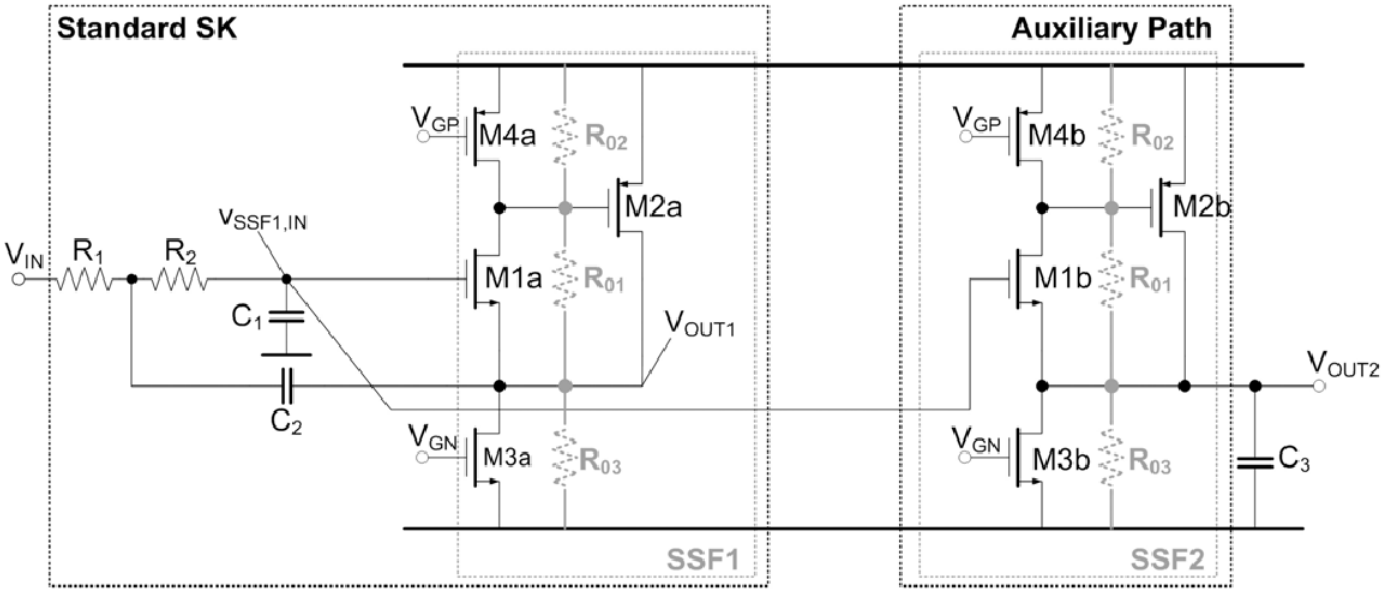


Fig. 1. SK single-ended generic scheme, with auxiliary path.

The total area occupancy is 0.12 mm^2

3.2-mW power consumption

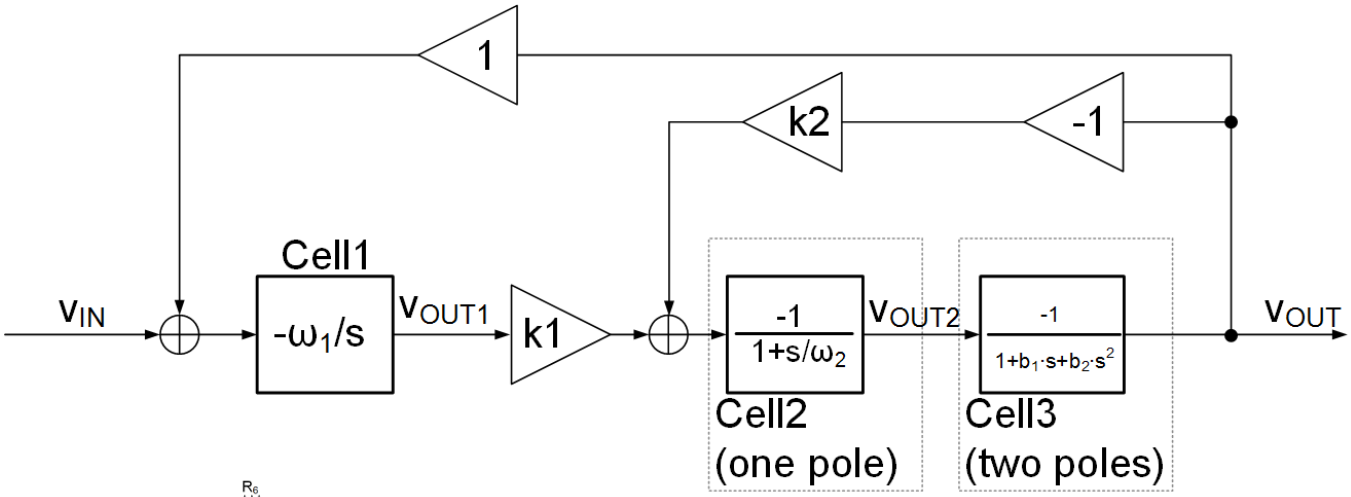
0.18u process

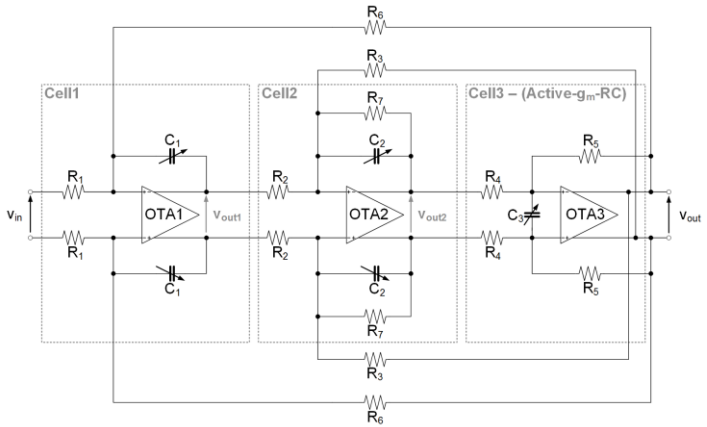
A 63-dB DR 22.5-MHz 21.5-dBm IIP3 Fourth-Order FLFB Analog Filter

Marcello De Matteis, Alessandra Pipino, Federica Resta, Alessandro Pezzotta, Stefano D'Amico, and Andrea Baschirotto

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 7, JULY 2017

Follow the Leader Feedback (a slight variant on the MLF approach)





Cell 3 Realized with Gm-RC stage of previous slide

Stay Safe and Stay Healthy !

End of Lecture 39

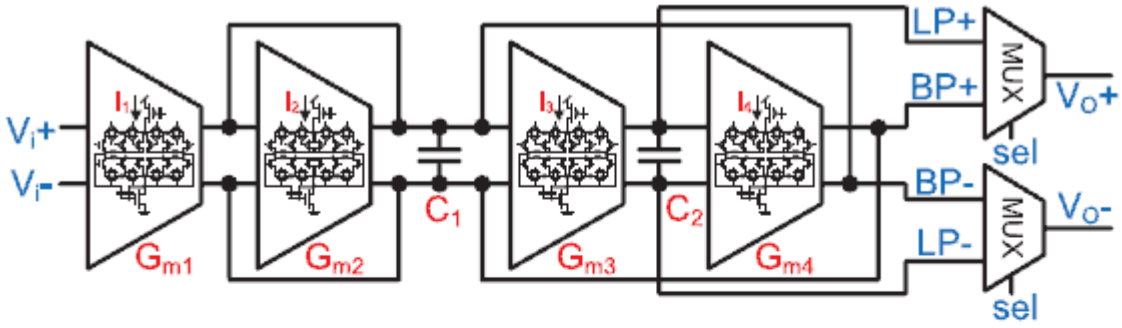
EE 508 Lecture 40

Some Recent Filter Structures

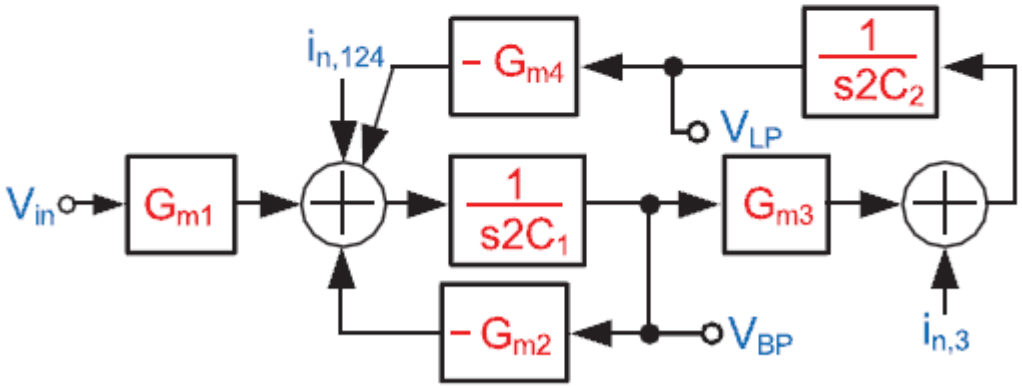
A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications

Sheng-Yu Peng, *Member, IEEE*, Yu-Hsien Lee, Tzu-Yun Wang, *Student Member, IEEE*, Hui-Chun Huang, Min-Rui Lai, Chiang-Hsi Lee, and Li-Han Liu

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, VOL. 65, NO. 2, FEBRUARY 2018

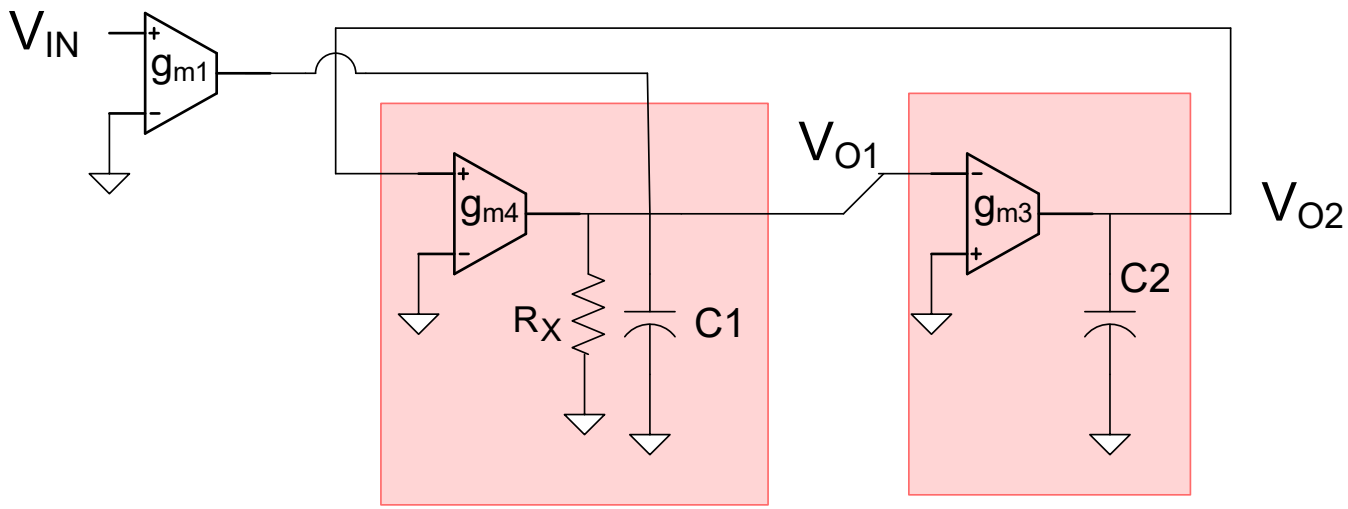


(a)



(b)

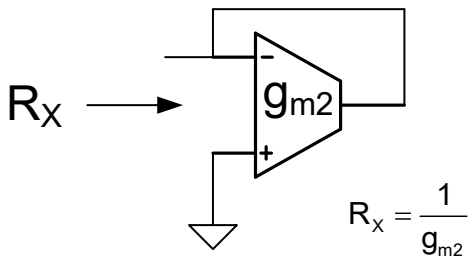
Recall the basic two-integrator loop



$$\left.\begin{aligned} V_{01}sC_1 &= G_X V_{01} + g_{m1}V_{IN} + g_{m4}V_{02} \\ V_{02}sC_2 &= g_{m3}V_{01} \end{aligned}\right\}$$

$$\frac{V_{01}}{V_{IN}} = \frac{s\dfrac{g_{m1}}{C_1}}{s^2 + s\dfrac{g_X}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$

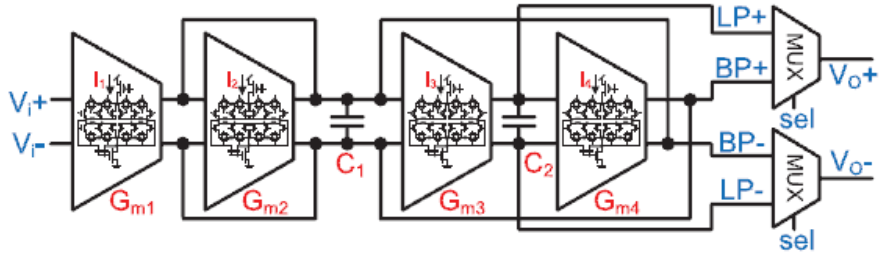
$$\frac{V_{02}}{V_{IN}} = \frac{\dfrac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\dfrac{g_X}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$



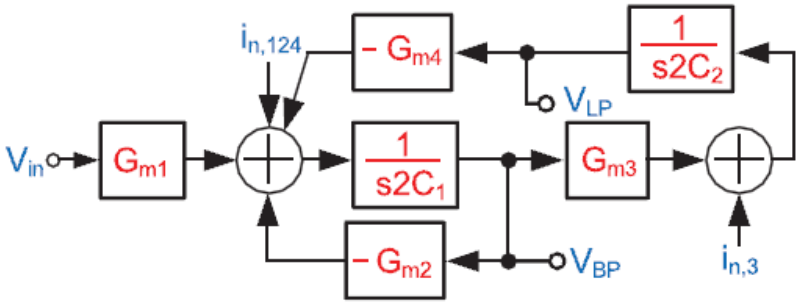
$$R_X = \frac{1}{g_{m2}}$$

$$\frac{V_{01}}{V_{IN}} = \frac{s\dfrac{g_{m1}}{C_1}}{s^2 + s\dfrac{g_{m2}}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\dfrac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\dfrac{g_{m2}}{C_1} + \dfrac{g_{m3}g_{m4}}{C_1C_2}}$$



(a)

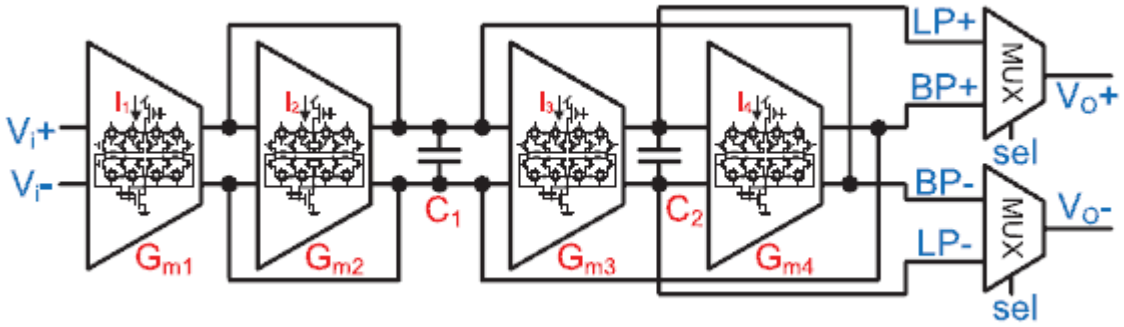


(b)

- This is a fully-differential implementation of the standard two-integrator loop
- MUX selects either LP or BP output

$$\frac{V_{01}}{V_{IN}} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\frac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$



- This is a fully-differential implementation of the standard two-integrator loop
- MUX selects either LP or BP output

$$\frac{V_{01}}{V_{IN}} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

$$\frac{V_{02}}{V_{IN}} = \frac{\frac{g_{m3}g_{m1}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}}$$

OTAs operate in weak inversion

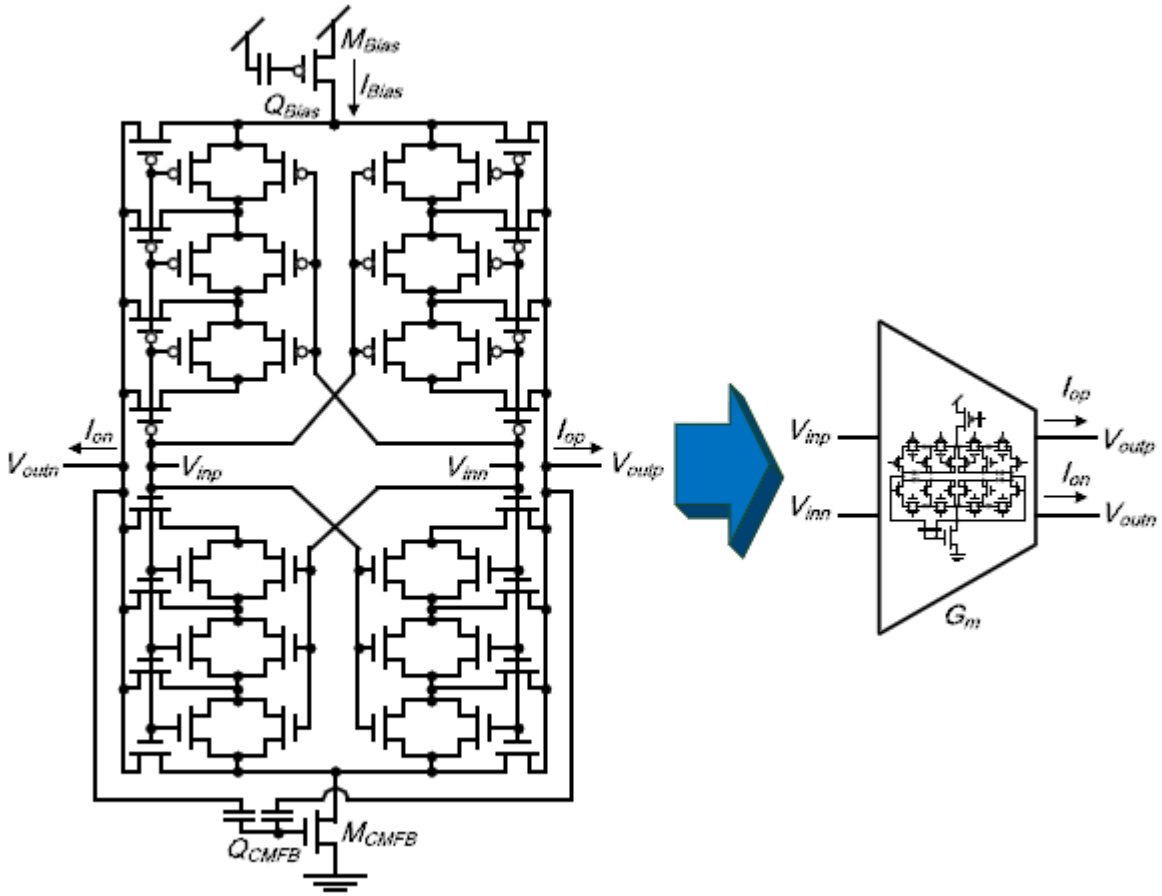
Adjust ω0 by changing tail currents – claim in excess of 5 decades of adjustment

Target 2Hz to 20KHz though claim can go much lower (claim to 10mHz range) and higher

Bias current adjusted by changing charge on floating gate transistor

Each biquad requires 0.12mm^2 of die area in 350nm process

Linearized OTA

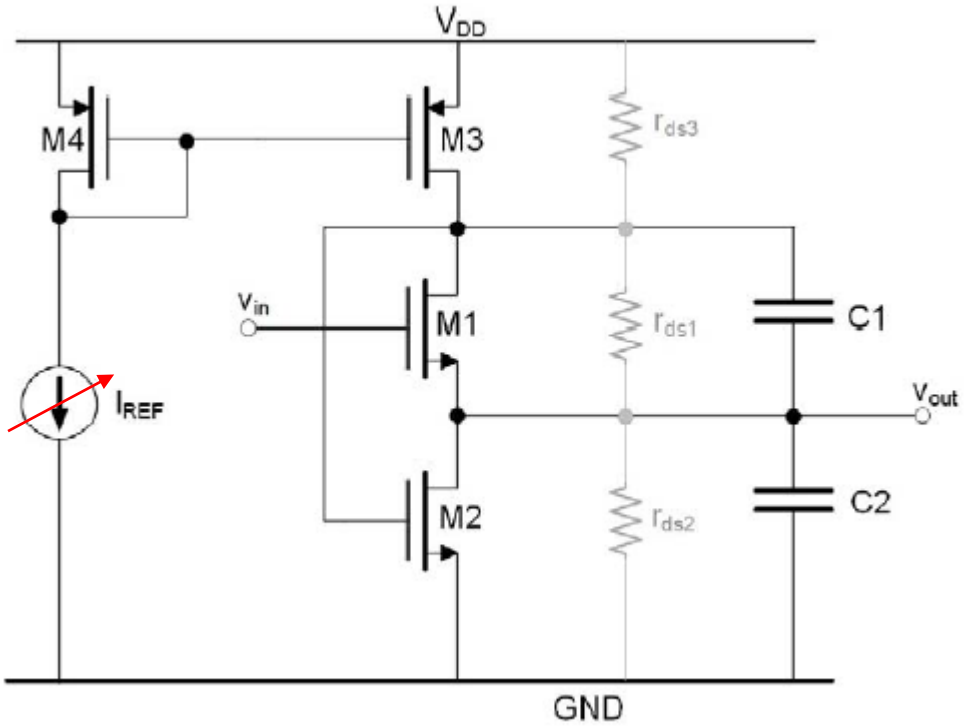


Used computer iteration to size devices in OTA
Good linearity and low power dissipation claimed

A 28nm-CMOS 100MHz 1mW 12dBm-IIP3 4th-order Flipped-Source-Follower Analog Filter

F. Fary1, M. De Matteis1, T. Vergine1,2 and A. Baschirotto1

ESSCIRC 2018

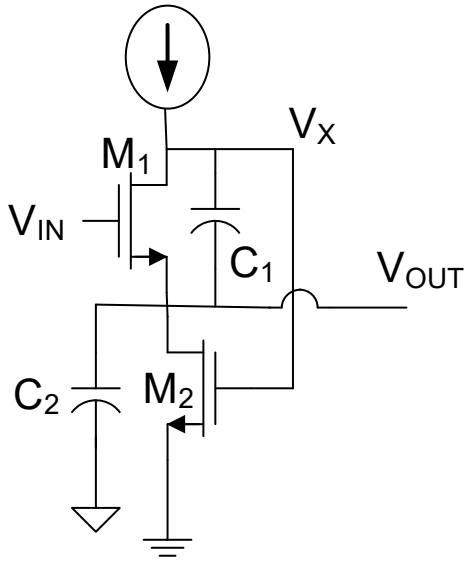


Flipped-Source-Follower NMOS Biquadratic Cell

Table 1 – Filter Design Paramters

Transfer Function		*4th-Order Low-Pass*	
dc-Gain		0dB	
Poles Frequency		100 MHz	
Cell A Q Factor	1.306	**Cell B Q Factor**	0.5412
Cell A g_{m1}- g_{m2}	1.8 mA/V	**Cell B g_{m1}- g_{m3}**	1.8 mA/V
Cell A - C_{1a}	4.8 pF	**Cell B - C_{1b}**	1.99 pF
Cell A - C_{2a}	1.75 pF	**Cell B - C_{2b}**	3.98 pF

A=0.026mm^2 for 4th order BW filter in 28nm process P approx. 1mW



$$\left.\begin{aligned} &V_{OUT}\left(sC_1+sC_2\right)+g_{m2}V_{GS2}-g_{m1}V_{GS1}=sC_1V_{GS2}\\ &V_{IN}=V_{GS1}+V_{OUT}\\ &V_{GS2}sC_1+g_{m1}V_{GS1}=V_{OUT}sC_1 \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}}=\frac{g_{m1}g_{m2}}{s^2C_1C_2+sC_1g_{m2}+g_{m1}g_{m2}}$$

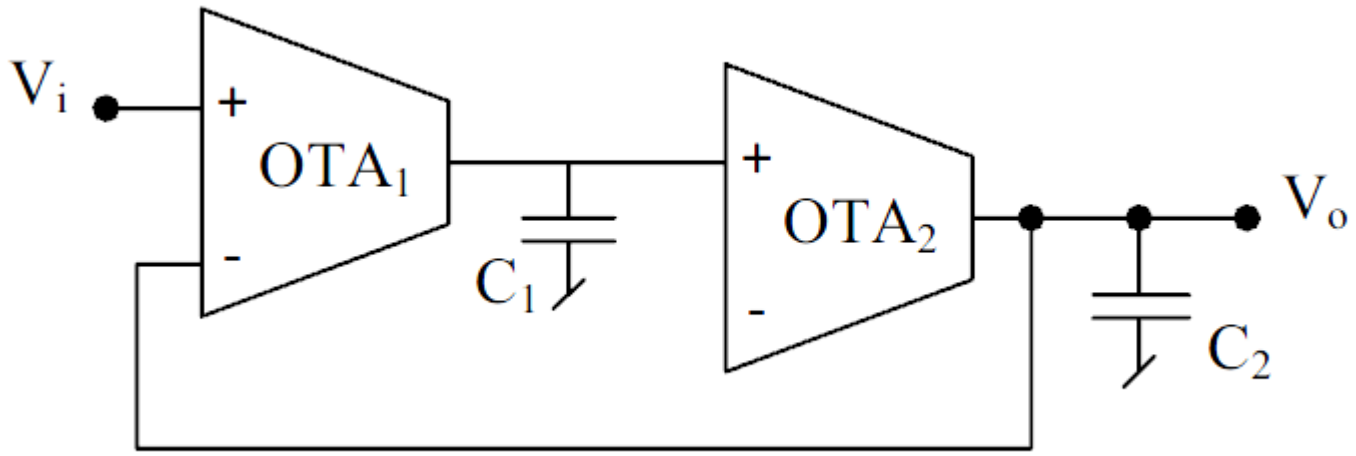
$$\omega_0=\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q=\sqrt{\frac{g_{m1}}{g_{\partial m2}}\frac{C_2}{C_1}}$$

A New Method to Design Multi-Standard Analog Baseband Low-Pass Filter

Ersin Alaybeyoğlu[1], Hakan Kuntman[2]

2017 10th International Conference on Electrical and Electronics Engineering (ELECO)



$$\frac{V_{LP}}{V_{in}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_1g_{m1} + g_{m1}g_{m2}}$$

$$w_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q = \sqrt{\frac{C_2g_{m2}}{C_1g_{m1}}}$$

10MHz – 40MHz

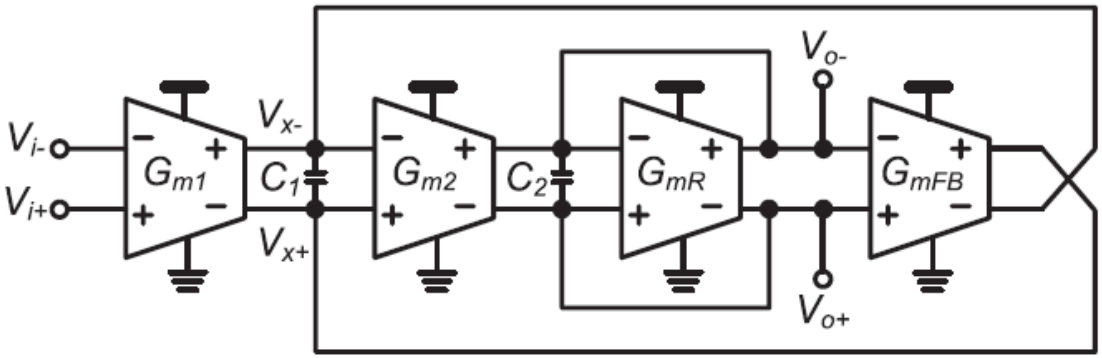
Projected Area 0.02mm^2 in 180nm proc

Low-Power *Gm–C* Filter Employing Current-Reuse Differential Difference Amplifiers

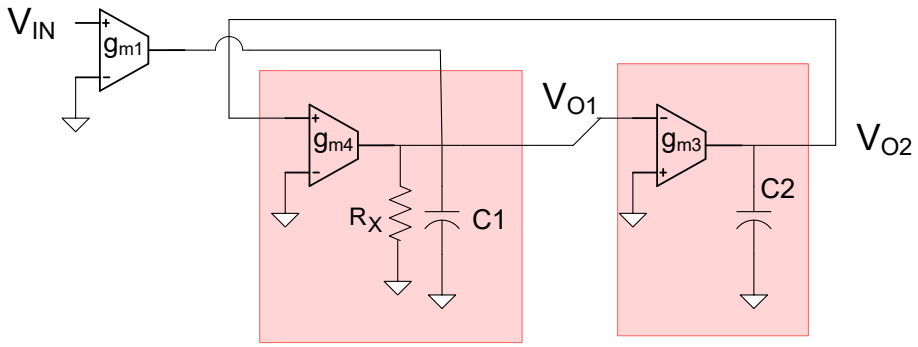
John S. Mincey, *Student Member, IEEE*, Carlos Briseno-Vidrios, *Student Member, IEEE*,
Jose Silva-Martinez, *Fellow, IEEE*, and Christopher T. Rodenbeck, *Senior Member, IEEE*

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 64, NO. 6, JUNE 2017

Typical Differential Implementation



Typical Single-Ended Implementation



Require 4 OTAs

Current-reuse Structures

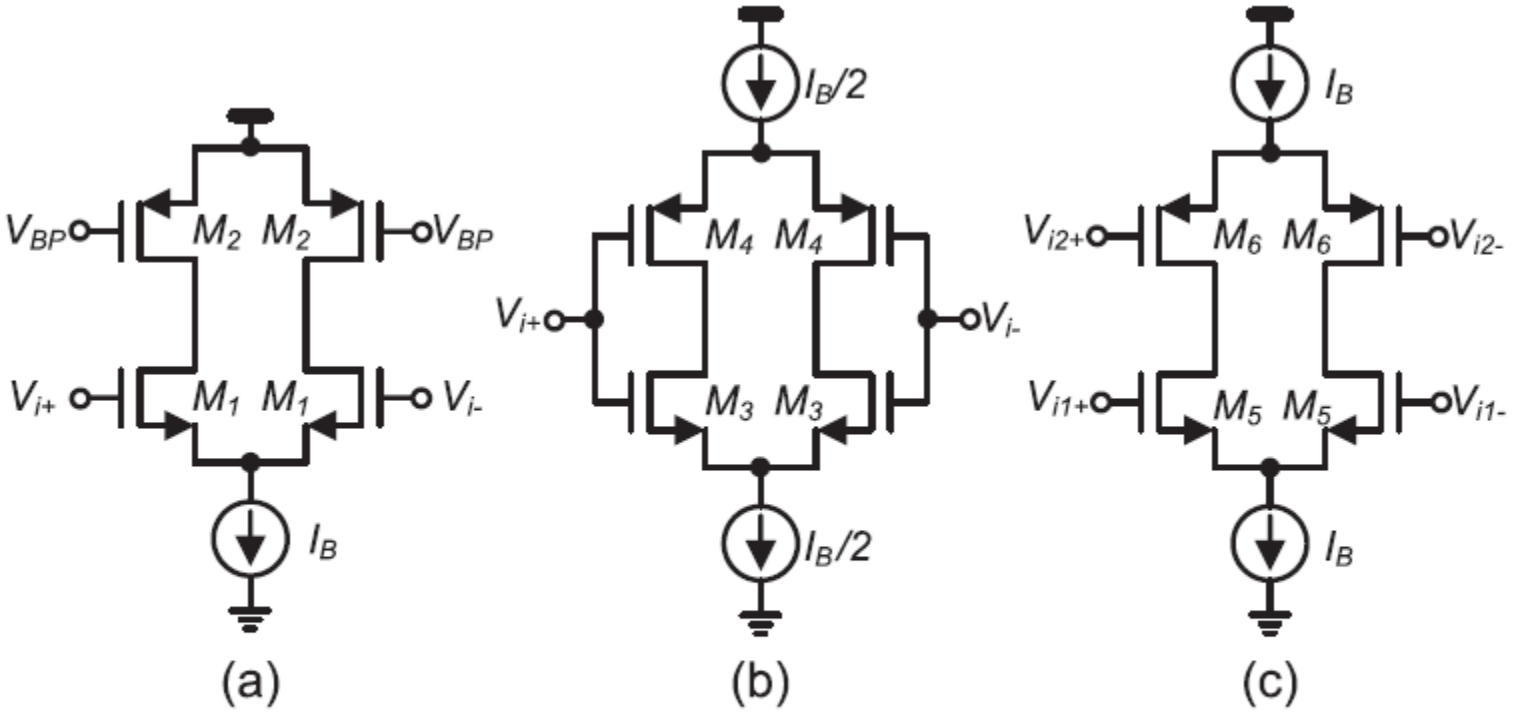


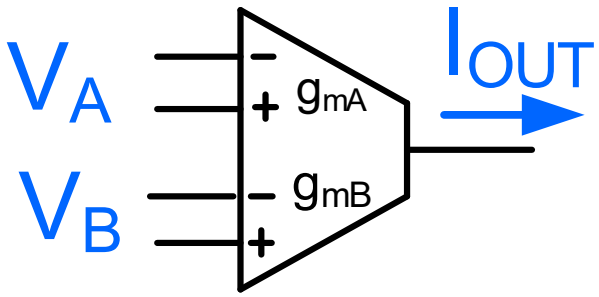
Fig. 3. (a) Conventional differential pair. (b) DDP using half the bias current. (c) Current-reuse DDA.

Dual Differential Pair: DDP

Dual Different Amplifier: DDA

Current Reuse offers potential for significant power reduction

Current-reuse Structures

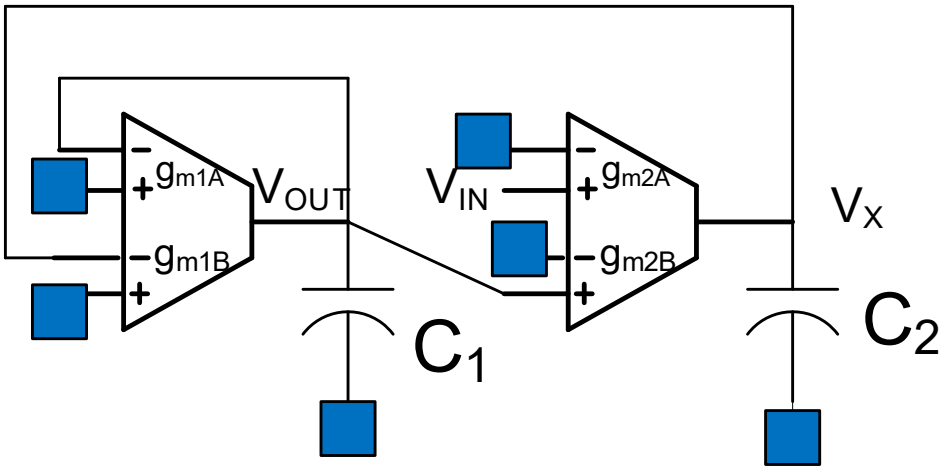


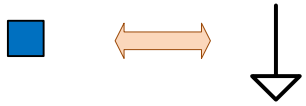
Dual input OTA

$$I_{OUT} = g_{mA} V_A + g_{mB} V_B$$

Current-reuse Structures

Consider:





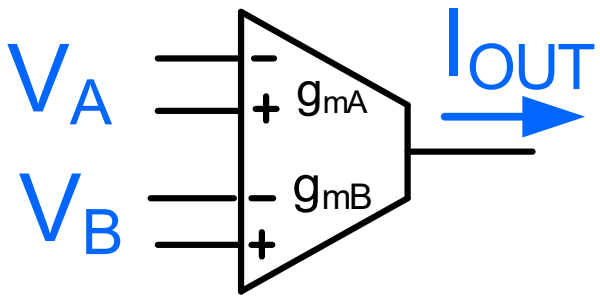
$$\left.\begin{aligned} V_{OUT}sC_1 &= -g_{m1A}V_{OUT} + g_{m1B}V_X \\ V_X sC_2 &= g_{m2B}V_{OUT} + g_{m2A}V_{IN} \end{aligned}\right\}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{g_{m2A}g_{m1B}}{\left(s^2C_1C_2 + sC_2g_{m1A} + g_{m1B}g_{m2B}\right)}$$

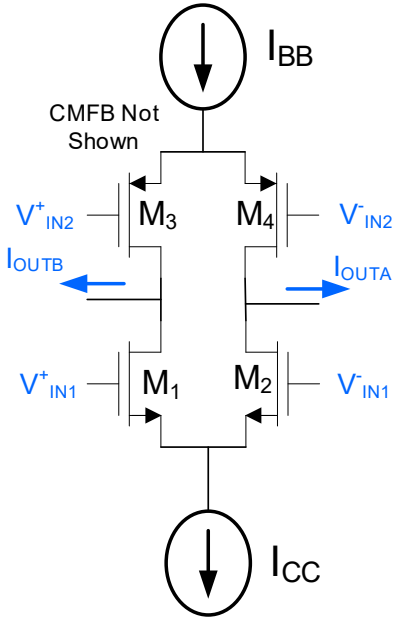
Realizes 2nd-order lowpass with just 2 OTAs

Current-reuse Structures

Dual input OTA



$$I_{OUT} = g_{mA} V_A + g_{mB} V_B$$

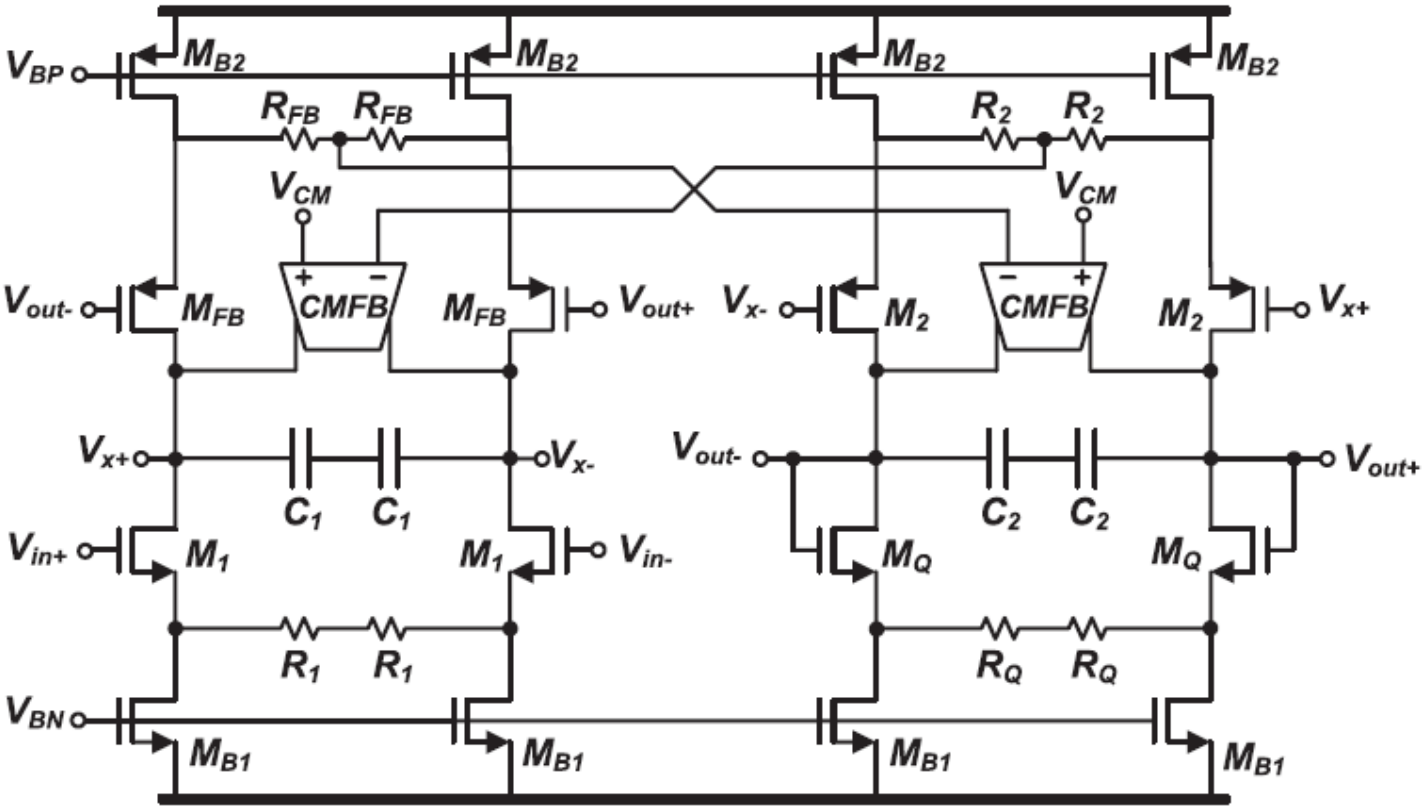


$$I_{OUTA} = g_{m2} V^-_{IN1} + g_{m4} V^-_{IN2}$$

$$I_{OUTB} = g_{m1} V^+_{IN1} + g_{m3} V^+_{IN2}$$

Current-reuse Structures

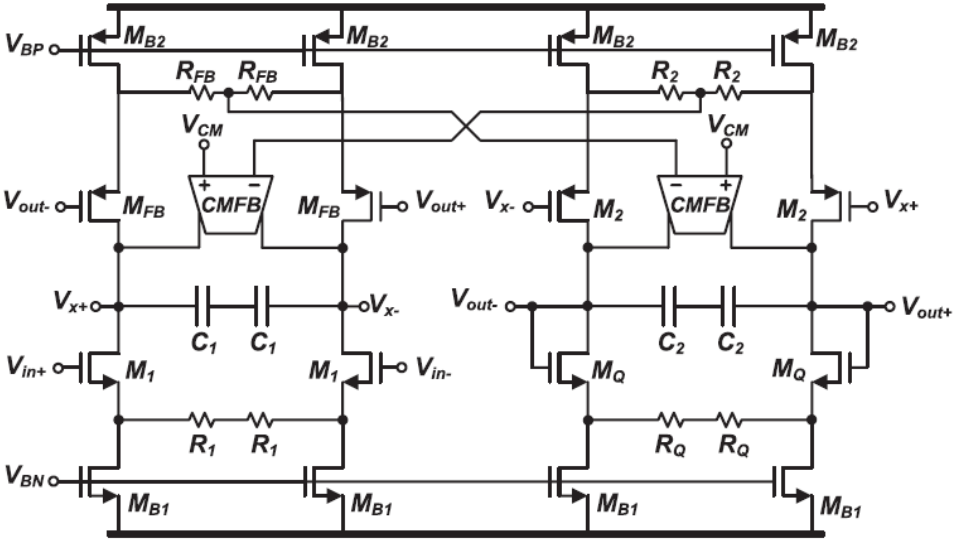
Dual input OTA



2nd Order Lowpass Biquad using Current-reuse OTA

Current-reuse Structures

Dual input OTA



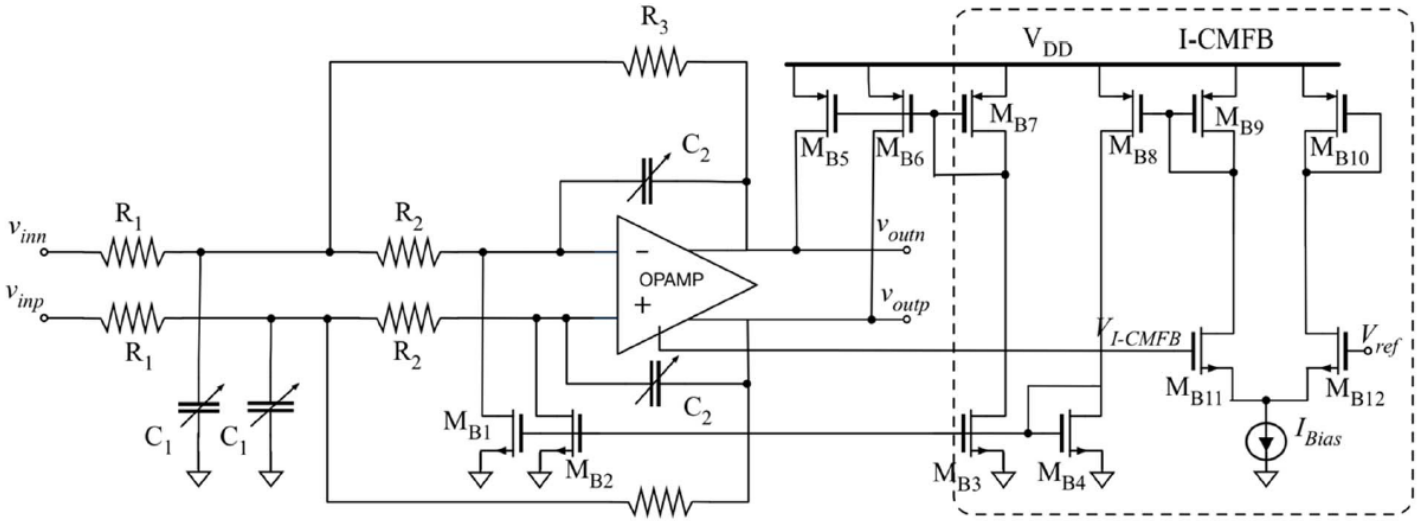
Sixth-order Butterworth G_m–C filter was fabricated

- 180-nm CMOS process
- total chip area of 0.21 mm^2
- 65MHz Band Edge
- 1.3mW/pole

A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology

F. Ciciotti, M. De Matteis, and A. Baschirotto

ISCAS 2018



$$H(s) \cong -\frac{R_3}{R_1} \cdot \frac{1}{1 + sC_2\left(R_2 + R_3 + R_2\frac{R_3}{R_1}\right) + s^2 C_1 C_2 R_2 R_3}$$

$$\omega_0 = \sqrt{\frac{1}{R_2 R_3 C_1 C_2}} \qquad Q = \sqrt{\frac{C_1}{C_2}} \frac{\sqrt{R_2 R_3}}{R_2 + R_3 + \frac{R_2 R_3}{R_1}}$$

A 0.9V 75MHz 2.8mW 4th-Order Analog Filter in CMOS-Bulk 28nm Technology

F. Ciciotti, M. De Matteis, and A. Baschirotto

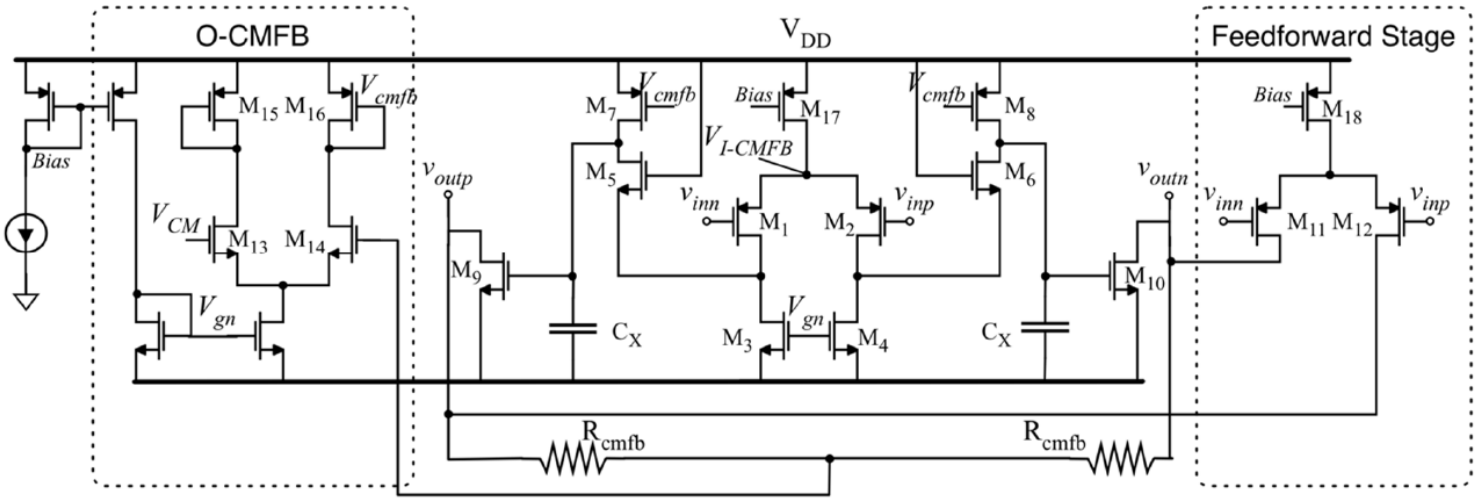


Fig. 2. Op Amp with feedforward compensation and O-CMFB circuit

CMOS 28nm process

4-bit capacitor arrays are used for frequency response programmability Filter covers the 40–105MHz range

0.7mW/pole

Area = 0.08mm^2

Stay Safe and Stay Healthy !

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